Celera MOTION
A Novanta Company

BiSS-C and SSI - An Overview

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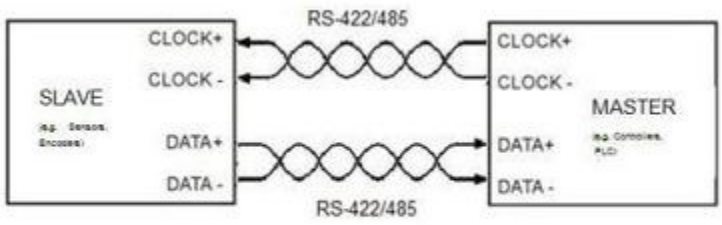
INTRODUCTION

Absolute position sensors measure the actual physical position within one revolution or within the range of linear travel. The resolution of these devices can exceed 20 bits and the interface of choice is a serial one. There are numerous serial interface implementations but only two, BiSS-C and SSI, are open and free from licensing expense. This paper gives an overview of BiSS-C and SSI with a summary of key differences.



SSI BLOCK DIAGRAM

BiSS and SSI are actually very similar – both use the concept of a master clocking data from a slave over a serial channel. The slave is the position sensor and the master is a servo drive or other controller. The sensor continuously updates the measured position in an output register. To read the sensor, the master initiates a series of clock pulses. When the slave detects the first clock pulse it freezes the output register and the most significant bit is output on the data line. The master continuous to generate clock pulses until all the bits in the output register have been transmitted. At this point the sensor resumes updating the output register.

The Clock and Data signals are differential on twisted-pair cable for improved immunity to electromagnetic interference. Electrical characteristics conform to RS-422/485 standards. The interface is inexpensive, reliable and capable of speeds up to 10 Mbits/sec (BiSS-C) on 10 meter cable. Much longer cables can be used at lower bit rates.

SSI

Synchronous Serial Interface (SSI) is point-to-point so slaves cannot be bussed together. SSI is uni-directional, data transmission being only from slave to master. It is therefore not possible for a master to send configuration data to a slave. Communication speeds are limited to 2 Mbits/sec.

Many SSI devices implement double transmissions to improve communication integrity. The master compares the transmissions to detect errors. Parity checking (Appendix) further improves error detection.

SSI is a relatively loose standard and many modified versions exist including the option for an incremental AqB or sin/cos interface. In this implementation absolute position is only read at startup.

BiSS-C

BiSS-C is the latest version of BiSS. Older versions (BiSS-B) are essentially obsolete. BiSS-C is hardware compatible with standard SSI but within each data cycle the master learns and compensates for line delays enabling 10 Mbit/s data rates and cable lengths up to 100 meters. Sensor data can comprise multiple "channels" so both position information and status can be transmitted in one frame. BiSS-C uses the more powerful CRC (Appendix) for detection of transmission errors.

BiSS-C is most often used unidirectionally like SSI. BiSS-C also supports bidirectional communication. Parameters can be exchanged without interrupting sensor data transmission. This is critical for digital control in motor feedback systems. BiSS-C recognizes the end of a cycle and uses the last recognized logic level on the clock line as a control/data bit for the sensor enabling parameter setting over several cycles.

BiSS-C is typically used point-to-point but also supports bussing. In the bus configuration all devices are connected in a chain. Each slave therefore has two connectors - BiSS-In and BiSS-Out. The clock line is pass-through so each slave receives the clock simultaneously. Data-Out of the first slave is connected to the master. Data-Out of the second slave is connected to the Data-In of the first slave and so on. In this way the data from all slaves is clocked out to the master in one continuous frame.

SUMMARY

As bidirectional transmission and bussing are not typically used in motion control applications, the primary advantages of BiSS-C are transmission speed and more robust error checking without the use of double transmissions. Fast data transfer means low latency – critical for high performance motion control. SSI is still used widely but BiSS-C, because of its advantages, continues to show significant growth in popularity.

APPENDIX

Parity There are two versions of parity checking: even and odd. In the case of even parity, the sensor counts the bits in the position data with a value of 1. If that count is odd, the parity bit value is set to 1, making the total count of occurrences of 1s in the whole set (including the parity bit) an even number. If the count of 1s is already even, the parity bit is set to 0. The master performs a similar check to ensure a data bit was not corrupted in the transmission.

CRC Cyclic Redundancy Check is a more powerful technique than parity checking which can fail to detect the corruption of multiple bits. The sensor applies a 16 or 32 bit polynomial to the position data that is to be transmitted and appends the result. The master applies the same polynomial to the data and compares its result with the result appended by the sender. If they agree, the data has been received successfully.