Veratus™ Advanced Signal Processing

TN-1004 | REV 160404

THE CHALLENGE

Modern, demanding motion control applications require high accuracy and stable velocity control. High resolution incremental optical encoders all operate on the basic principal of counting a recurring diffraction pattern. Long range accuracy describes the total error seen across the full range of motion while short range accuracy describes the error of the interpolated signal. This short range error is referred to by several names: interpolation error, cyclical error, intra-fringe error, sub-divisional error (SDE), etc. All of these terms denote the same concept, namely, how accurately is the fundamental analog signal being divided down into smaller increments of resolution.

Many encoder products made by MicroE and other encoder companies require a calibration procedure during setup using either a separate alignment tool or push-button technique during installation. This procedure calculates static correction coefficients to help improve the fidelity of the raw analog encoder signal prior to interpolation. One disadvantage of this technique is that it slows down and complicates the installation procedure. Another is that the correction coefficients are calculated based only on a small sampling of the scale on the assumption it will be representative of the entire range of motion. Thirdly, these corrections often are done in the digital domain making it impossible to offer a corrected, high fidelity analog output to the customer.

THE SOLUTION: VERATUS™ ADVANCED SIGNAL PROCESSING (AUTO CALIBRATION)

An extremely convenient and powerful way to observe the fidelity of analog sin/cos signals is with Lissajous figures, where differential sin and cos are displayed in an X-Y plot. In this format, one period of the sin and cos signals are displayed as a single trip around this circle. For the majority of MicroE encoders, this distance is 20um as determined by the line pitch of our diffractive grating. The closer the sin and cos signals are to perfect mathematical sinusoidal functions, the closer this display comes to a perfectly round circle centered on the origin. A perfect circle would result in zero SDE. Interpolation is simply the process of dividing this circle into equal segments using an arc-tan calculation in software. For 200nm resolution, the circle would be divided equally into 100 segments of 3.6°. As with any optical encoder, there are error sources in the optics, electronics, and grating pattern that prevent the sin and cos from being mathematically perfect.

Figure 1: Lissajous Plot

While there are a variety of ways the Lissajous can be distorted from perfect, the most significant sources of SDE are gain mismatch, DC offset mismatch and phase shift between the sin and cos. Figure
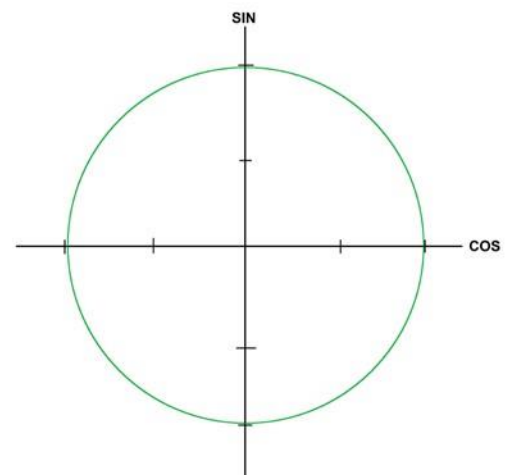
2 below shows and example of a gain mismatch where the amplitude of the cos signal is smaller than the sin signal. Figure 3 is an example of a DC offset mismatch between the Sin+ and Sin-
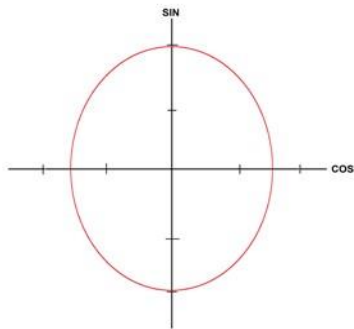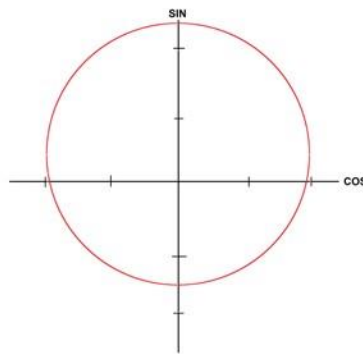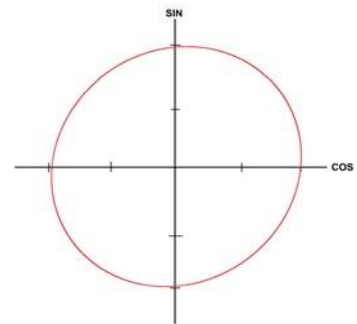

| Fig. 2: Gain | Fig. 3: Offset | Fig. 4: Phase |

signals which has forced the circle off center. Figure 4 shows an example of a phase difference between Sin and Cos being shifted away from 90°. The Veratus family of encoders employs real-time accuracy corrections, in the analog domain, so the encoder with analog sin/cos outputs delivers the specified accuracy, repeatability and noise performance without any other customer supplied signal processing or corrective circuitry. In fact, additional signal processing may only worsen the specified performance. The digital output versions also benefit from the analog signal processing because it is done before the internal A-quad-B generator inputs.

The internal analog control loops are:

- <u>Vector magnitude loop</u>: adjusts the light source current so the vector magnitude is 1V$_{pp}$ into 120Ω.
- <u>Sin/Cos offset loops</u>: adjust the offset of the Sin/Cos signals so the Lissajous is centered.
- <u>Sin tracking Cos loop</u>: adjusts the gain balance between Sin and Cos so that the Lissajous is round.
- <u>Output common mode voltage loop</u>: sets the output common mode voltage of Sin/Cos to 1.9VDC

The control loop bandwidths are carefully chosen so as to track errors caused by alignment, temperature and time, thus minimizing SDE but not causing repeatability issues by arriving at different corrections when the encoder travels in one direction versus the other. The control loop parameters are saved to internal memory so that the loops can resume at their previous operating points whenever the encoder is power cycled, therefore avoiding any accuracy settling time issues at start-up. The settling time can be problematic in other approaches because the offset and gain tracking loops, by their very nature are spatial, which forces the customer to traverse specified distances before the loops are settled and producing accurate corrections. The phase between sin and cos is controlled in Veratus by the geometry of the optics. Extensive factory testing has shown that no active phase compensation is necessary.

For Veratus, the index reference mark is encoded in a series of parallel stripes with the main track so that index phasing does not change with encoder $_{\theta z}$ misalignment. Furthermore, it is encoded such that the Index Window signal is true and centered when Sin=Cos for the analog version and true when A=B=1 for the digital version. Consequently, the customer does not have to adjust or calibrate the encoder in any way, other than to arrive at a healthy LED indication to ensure that the encoder meets all specified requirements and index phasing.

The customer need only to install the encoder, align it using the supplied shim or align it until a "blue" LED indication, then move ~1 inch (25mm), one time only after installation, to achieve specified accuracy.